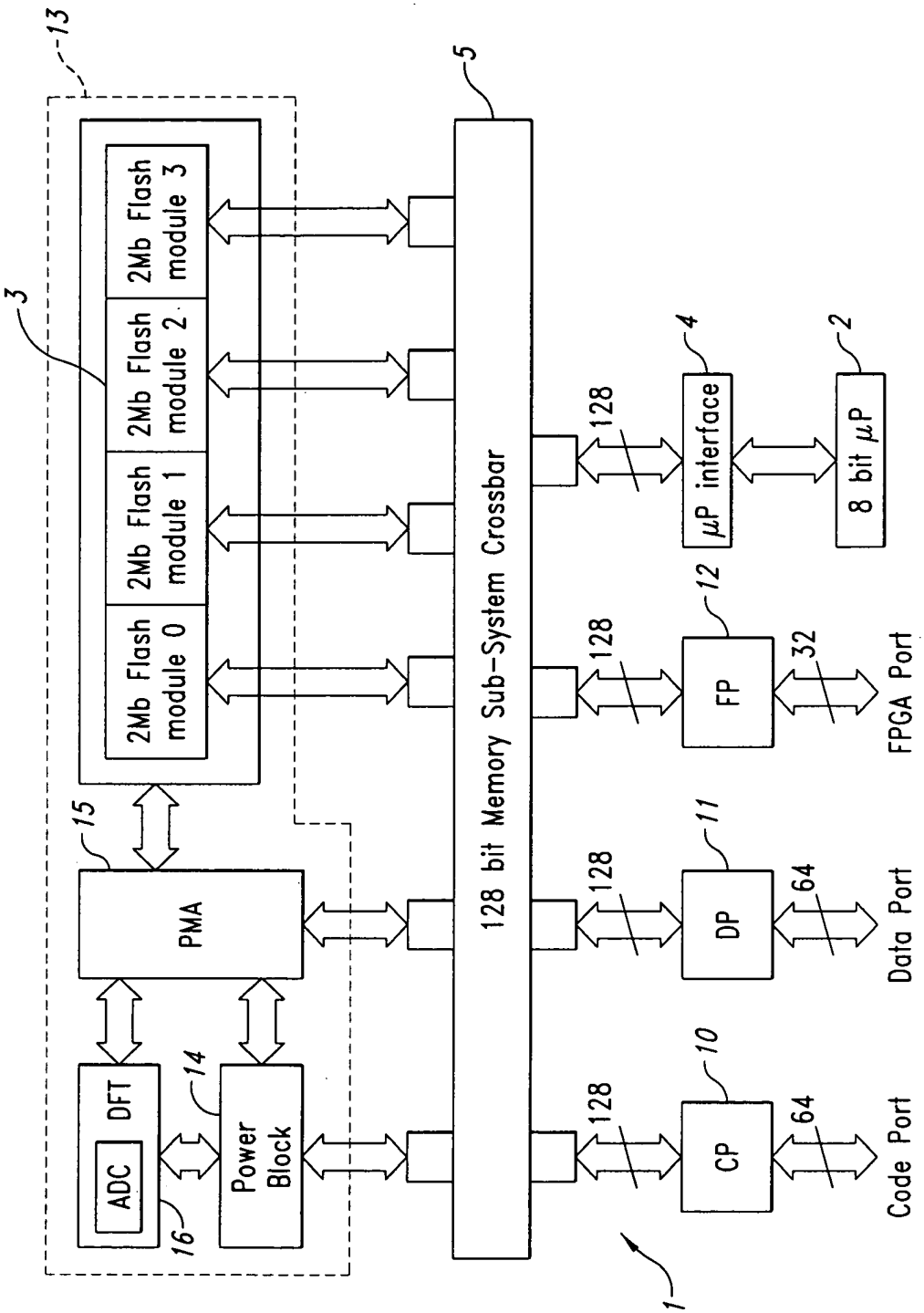
13
5
3
2Mb Flash module 3
2Mb Flash module 2
2Mb Flash module 1
2Mb Flash module 0
128 bit Memory Sub-System Crossbar
128
4
μP interface
2
8 bit μP
12
FP
32
FPGA Port
15
PMA
11
DP
64
Data Port
DFT
ADC
14
Power Block
10
CP
64
Code Port
16
1

FIG. 1

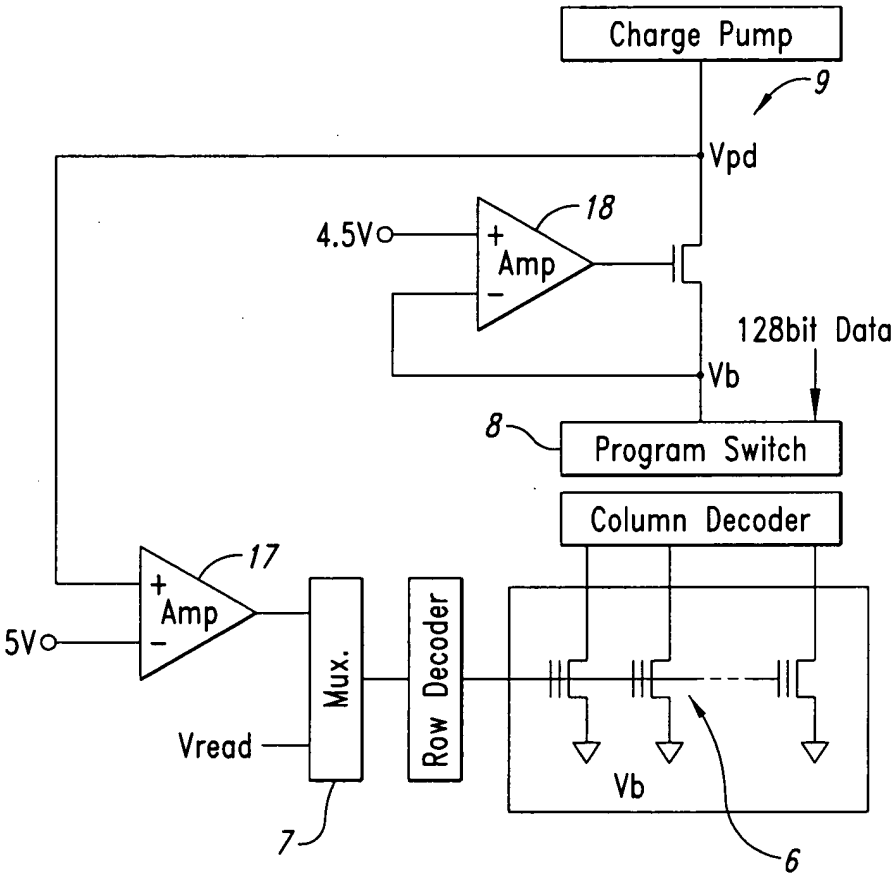
Charge Pump
9
Vpd
4.5V
18
+
Amp
−
128bit Data
Vb
8
Program Switch
Column Decoder
17
+
Amp
−
5V
Mux.
Row Decoder
Vread
Vb
7
6

FIG. 2

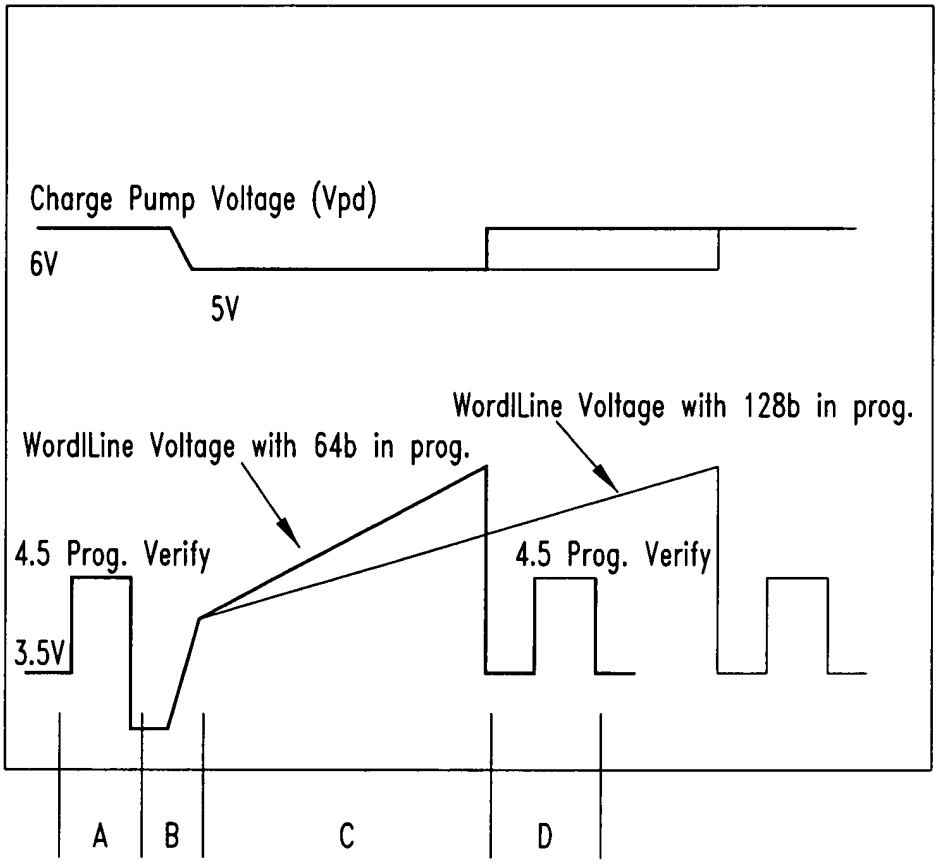
Charge Pump Voltage (Vpd)
6V
5V
WordlLine Voltage with 128b in prog.
WordlLine Voltage with 64b in prog.
4.5 Prog. Verify
4.5 Prog. Verify
3.5V
A
B
C
D

FIG. 3

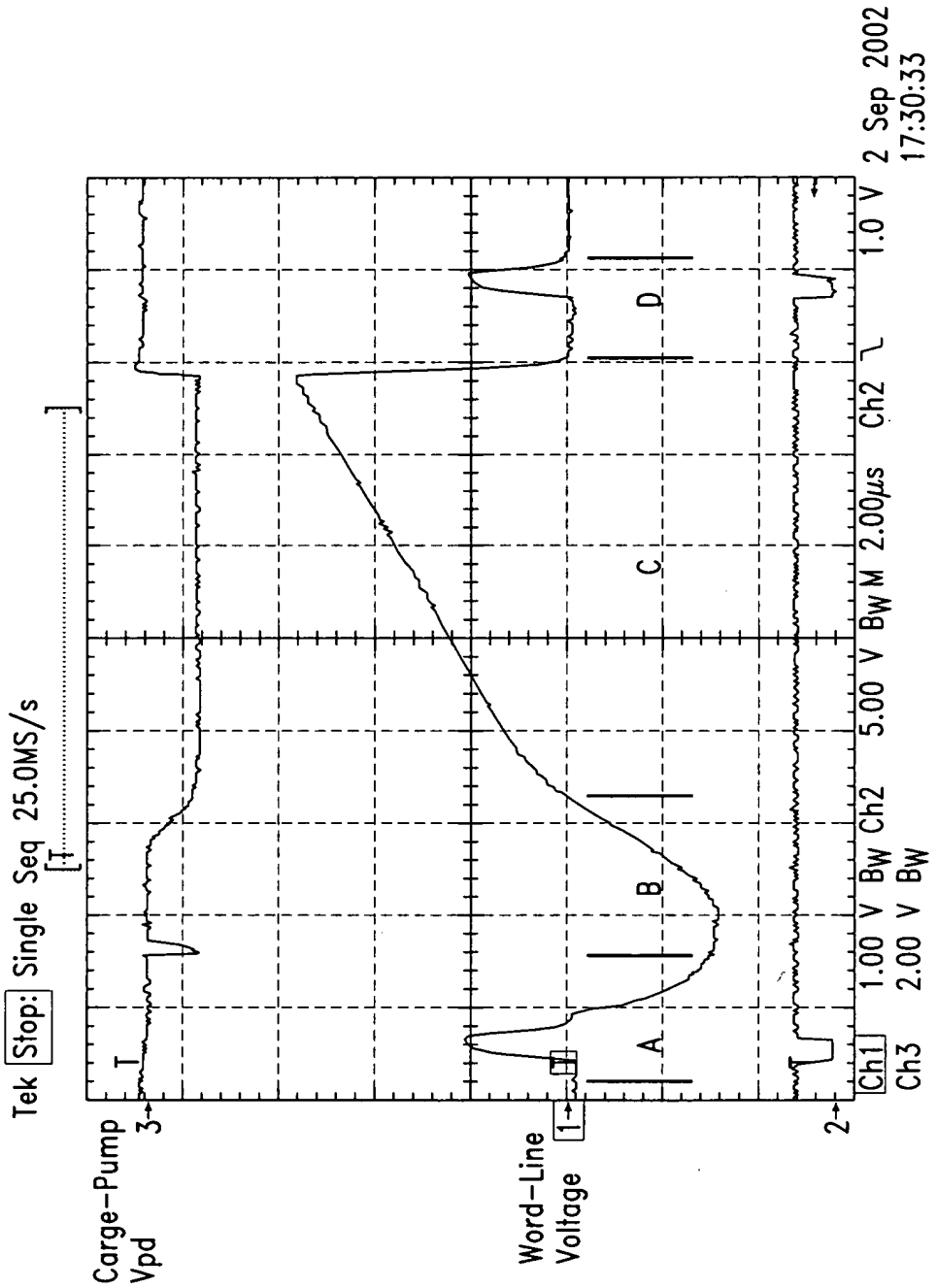
Tek Stop: Single Seq 25.0MS/s
Carge-Pump
Vpd
Word-Line
Voltage
Ch1 1.00 V Bw Ch2 5.00 V Bw M 2.00µs Ch2 1.0 V
Ch3 2.00 V Bw
2 Sep 2002
17:30:33
A
B
C
D

FIG. 4

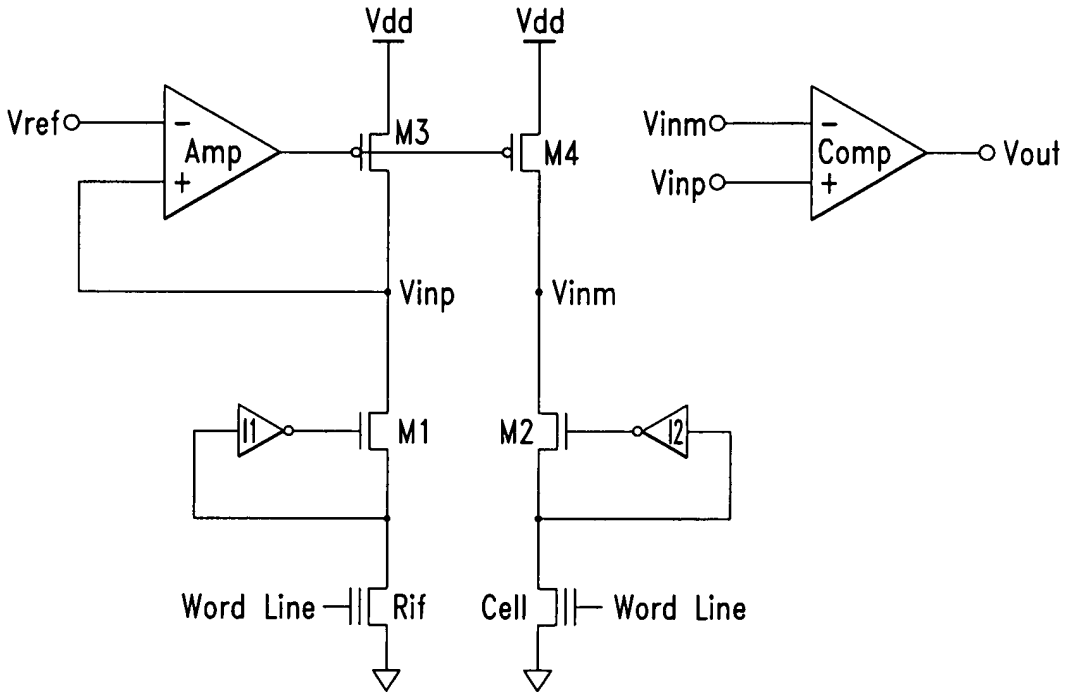
Vdd
Vdd
Vref
Amp
M3
M4
Vinm
Comp
Vout
Vinp
Vinp
Vinm
I1
M1
M2
I2
Word Line
Rif
Cell
Word Line

FIG. 5

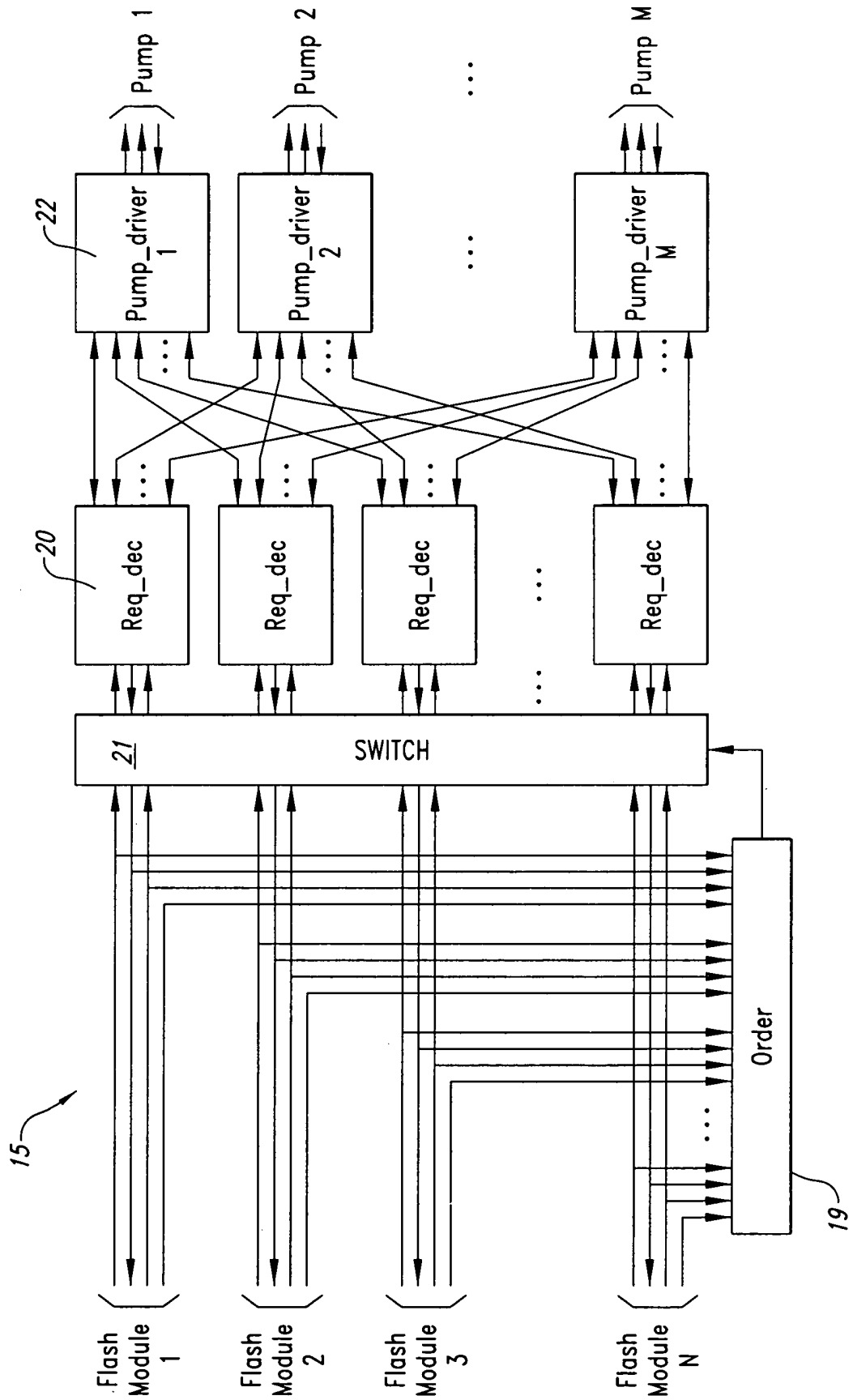
Pump 1
Pump 2
Pump M
22
Pump_driver 1
Pump_driver 2
Pump_driver M
20
Req_dec
Req_dec
Req_dec
Req_dec
21
SWITCH
Order
19
15
Flash Module 1
Flash Module 2
Flash Module 3
Flash Module N

FIG. 6

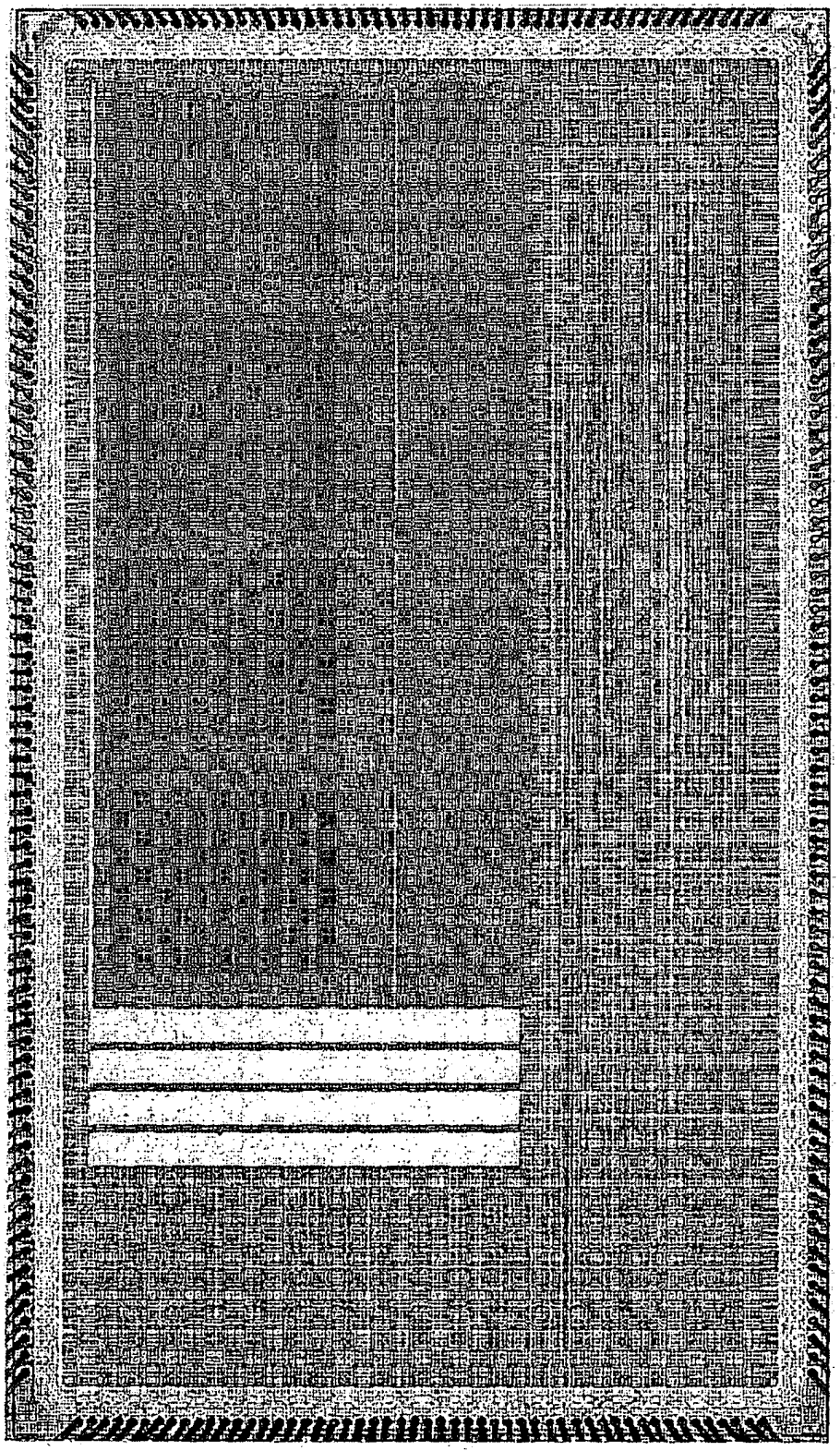

FIG. 7